STRUCTURE AND METHOD FOR RESURF DIODES WITH A CURRENT DIVERTER

TECHNICAL FIELD

This invention generally relates to Smart Power integrated circuits and, more particularly, to means and methods for reducing substrate leakage currents associated with RESURF diodes employed in such integrated circuits.

BACKGROUND

There are many integrated circuit (IC) applications today in which a diode is formed by using a source region and gate terminal of a metal oxide semiconductor field effect transistor (MOSFET) shorted together forming an anode (or cathode), and what would ordinarily be the drain region of the MOSFET acting as the cathode (or anode) of the diode. Such structures are particularly useful in connection with RESURF devices. "RESURF" is an abbreviation standing for "reduced surface field." RESURF devices and method are described for example, in U.S. Pat. No. 6,882,023 B2 to Khemka et al and U.S. Pat. No. 6,747,332 B2 to de Fresart et al.

A known RESURF diode device is illustrated in FIG. **1**, which shows a simplified schematic cross-section through double RESURF MOSFET diode device **20**. RESURF MOSFET structures and methods are well known in the art and much used in power ICs. RESURF diode device **20** comprises P substrate **22**, N-type buried layer (NBL) **24** overlying substrate **22**, P-epi region **26** overlying NBL **24**, P-buried region **28** typically implanted within P-epi region **26**, N-well region **30** located between P-buried region **28** and surface **35**, P-body region **32** extending into P-epi region **26** from surface **35** and laterally separated from N-well region **30** by channel region **27**, N+ sinker region **34** extending from surface **35** through P-epi region **26** to NBL **24**, N+ contact region **36** at surface **35** in N+ sinker region **34** for making contact to NBL **24** via N+ sinker region **34**, P+ (e.g., anode) region **38** in P-body region **32** laterally separated from N+ contact region **36** by oxide (OX) isolation region **40**, MOS gate **42** located over surface **35** above portion **33** of P-body region **32** extending laterally from P+ anode region **38** across channel region **27** and portion **31** of N-well region **30** and separated therefrom by thin gate oxide **43** on surface **35**. Isolation oxide (OX) region **44** is provided vertically extending from surface **35** into N-well region **30** and laterally extending approximately from edge **42-1** of gate **42** to N+ cathode region **46** in N-well region **30** at surface **35**. Connection **39** with lead **29** coupling P+ anode region **38** and gate **42** forms the anode contact of RESURF diode device **20** and connection **47** to N+ region **46** forms the cathode contact of RESURF diode device **20**. Connection **41** is typically provided tying BL contact **37** to cathode connection **47**.

FIG. **2** is simplified electrical equivalent circuit **50** of diode **20** of FIG. **1**. Equivalent circuit **50** comprises PN diode **52** and PNP parasitic transistor **54** inherently present in RESURF diode device **20** of FIG. **1**. PN diode **52** is provided by anode region **38** with contact **39** in P-body **32** and cathode region **46** with contact **47** in N-well **30**. Parasitic PNP transistor **54** is provided by P-epi region **26**, P-body **32** and contact region **38** that act as emitter **55**; NBL **24** that acts as base **56**; and P substrate **22** that acts as collector **57**. Base **56** is coupled to cathode contact **47** via N+ sinker region **34**, N+ contact region **36** and connection **41**. While the arrangement of FIGS. **1-2** provides a convenient diode that is easily manufactured in connection with RESURF integrated circuits, it suffers from a number of well-known disadvantages. For example and not intended to be limiting, parasitic transistor **54** provides a leakage current path to substrate **22** as the forward bias across diode **52** is increased. This is undesirable and can degrade overall performance of the integrated circuit within which the diode of FIGS. **1-2** is incorporated. Thus, there continues to be a need for improved diodes that are process compatible with RESURF and other types of integrated circuits.

Accordingly, it is desirable to provide an improved integrated circuit diode structure and method that is compatible with integrated circuit technology, especially MOSFET integrated circuit technology and most particularly RESURF type MOSFETs. In addition, it is desirable that the improved diode structure and method be achievable with little or no change in established manufacturing processes, preferably, accomplished merely by modification of the masking layer(s) used for fabrication of the integrated circuits without having to add additional process steps. Furthermore, other desirable features and characteristics of the invention will become apparent from the subsequent detailed description and the appended claims, taken in conjunction with the accompanying drawings and the foregoing technical field and background.

BRIEF DESCRIPTION OF THE DRAWINGS

The invention will hereinafter be described in conjunction with the following drawing figures, wherein like numerals denote like elements, and

FIG. **1** is a simplified schematic cross-section through a known double RESURF diode device;

FIG. **2** is a simplified electrical equivalent circuit of the diode device of FIG. **1**;

FIG. **3** is a simplified schematic cross-section through a RESURF diode device according to a first exemplary embodiment of the invention;

FIG. **4** is a simplified electrical equivalent circuit of the diode device of FIG. **3**;

FIG. **5** is a simplified schematic cross-section through a RESURF diode device according to a further exemplary embodiment of the invention;

FIG. **6** is a simplified electrical equivalent circuit of the diode device of FIG. **5**;

FIG. **7** is a simplified schematic cross-section through a further known RESURF diode device;

FIG. **8** is a simplified electrical equivalent circuit of the diode device of FIG. **7**;

FIG. **9** is a simplified schematic cross-section through a RESURF diode device according to a still further exemplary embodiment of the invention;

FIG. **10** is a simplified electrical equivalent circuit of the diode device of FIG. **9**;

FIG. **11** shows plots as a function of forward current of the ratio of substrate current (Isub) to diode current (Ic) for diode devices of the prior art and the invention of the type illustrated in FIGS. **1** and **3**; and

FIG. **12** shows plots as a function of forward current of the ratio of diode current (Ic) to substrate current (Isub) for diode devices of the prior art and the invention of the type illustrated in FIGS. **7** and **9**.

DETAILED DESCRIPTION

The following detailed description is merely exemplary in nature and is not intended to limit the invention or the application and uses of the invention. Furthermore, there is no intention to be bound by any expressed or implied theory